International Journal of Engineering Science Invention Research & Development; Vol. III, Issue X, April 2017
www.ijesird.com, e-ISSN: 2349-6185

DESIGN AND ANALYSIS OF LOW POWER AND LESS AREA FLIP-FLOP IN SEQUENTIAL CIRCUITS

Leo joseph[1] , Vigneswari[2]
M.E VLSI Design[1], Asst Proff[2], Department of ECE,JCT College of engg and technology, Coimbatore
Leojoseph1991@gmail.com[1]

***Abstract*-The motto of this proposal is principally focused on Timing Elements in digital circuits. Initially a low-power and area-efficient shift register using pulsed latches are designed. It resolves timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals. Even though Implicit and Explicit Flip-flop design is present design It is an alternative of the conventional single pulsed clock signal. Flip-flops are perilous timing elements in digital circuits which have a huge influence on the circuit speed and power consumption. The performance of flip-flop is a significant element to regulate the efficiency of the entire synchronous circuit. For efficient low power and less area flip flop design the H-spice and T-spice tools are used. Razor flip flop with GDI technique also involved in the proposing technique. This will guaranty the high efficient Performance.**

***Keywords:* GDI,DET,SETFFs, flip-flop, pulsed clock, pulsed latch, shift register.**

I. INTRODUCTION OF LOW-POWER AND AREA-EFFICIENT SHIFT REGISTERS USING PULSED LATCH

Sequential logic circuits, such as registers, memory elements, counters, etc., are heavily used in the implementation of very large scale integrated (VLSI) circuits. Power consumption of very large scale integrated VLSI chips is growing to be an increasingly crucial problem as chip densities increase. Therefore the improvement of such circuits such as a decrease in power consumption, without weakening other characteristics, is of prime Importance to the VLSI industry. Currently, several designs are described in CMOS technology.The new value is stored when the pulse of the clock signal occurs[1]. The state of a flipflops can change only during a clock pulse transition. Double edge trigger flip-flop (DET), which can be both triggered at the rising edge and falling edge of a clock, since they can maintain the same throughput as single edge-triggered flip-flops (SETFFs) while only using half of the clock frequency. Compared to rising edge-triggered flip-flop which process data only at the rising transition of the clock, the DET doubles the rate of data processing or, alternatively halves the clock rate thereby, either increasing the data throughput or reducing power consumption in the clock circuit respectively. Thus reduced power and high-speed operation is possible. DETFFs have been applied to low-power application-specific integrated circuit (ASIC) designs, and also have been employed in high-level synthesis as the primary storage.

II. OBJECTIVE OF THE WORK

In VLSI low power circuit design the efficiency is important consideration which is increased by using double edge triggered flip flop. Another suitable technique is clock gating it reduces the dynamic power of idle modules or idle cycles[2],[3]. By incorporating clock gating with DETFFs to further reduce dynamic power consumption introduces an asynchronous data sampling. For a clock-gated system, the internal clock controls the gated circuits.

During the gated periods, the internal clock is separated from the global clock. If the internal clock is out of phase with the global clock when the gating signal is de-asserted, then the internal clock signal switches immediately to match the global clock. This internal clock switch is extra and not synchronized with the external clock, which creates an asynchronous data sampling, evidenced by the

output changing between clock edges. Asynchronous data sampling shares the same root cause, namely the discontinuity between the global and internal clock[6].The proposed methods are designed in T-spice,H-spice Tanner tools 13v were used. The performance parameters are calculated based on the obtained waveforms.

III. MOTIVATION OF THE WORK

This work presents technique of Area and time mismatching reduction in synchronous design circuit. In order minimize power consumption the three different clock gated dual edge triggered flip-flops are proposed by eliminating asynchronous data sampling because it introduces the data miscommunication error. Two approaches are designed to filter out the asynchronous data sampling by only resuming the connection between the global clock and the internal clock when they are in phase. The third approach avoids the asynchronous data sampling by synchronizing the clock-gating signal with the global clock.

A. DUAL-EDGE TRIGGERED STORAGE ELEMENTS AND CLOCKING STRATEGY FOR LOW

This project introduced advanced two DET flip-flops are described that allow clock frequency reduction while maintaining comparable timing overhead and clock load to the conventional SETSE.The one methods is DET conditional pre charge flip-flop (DE-CPFF) is presented, based on the generation of a transparency window after each clock edge, and reduction of the internal switching activity.

IV. LOW-POWER CLOCK BRANCH SHARING DOUBLE-EDGE TRIGGERED FLIP-FLOP

Double-edge triggered flip-flops employs a clock branch-sharing scheme to reduce the number of clocked transistors in the design[7]. The newly proposed Design also employs conditional discharge and split-path Techniques to further reduce switching activity and short-circuit Currents, respectively.

The clock system which consists of the clock distribution network and timing elements (flip-flops and latches),is one of the most power consuming components in a VLSI system. It accounts for 30% to 60% of the total power dissipation in a system As a result ,reducing the power consumed by flip-flops will have a deep impact on the total power consumed .Voltage scaling is the most effective way to decrease power consumption, since power is proportional to the square of the voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage to increase exponentially besides supply voltage scaling, double-edge clocking can be used to save half of the power on the clock distribution network.

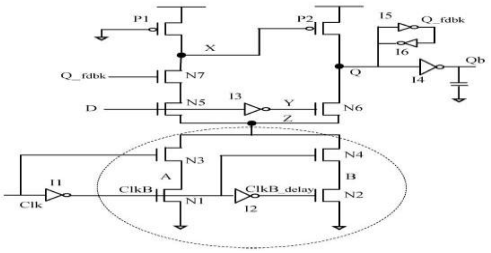


Figure 1 CBS flip-flop

In this case, the falling Transition of the input will cause the pull down network of the second stage to be ON and, thus, forcing the output nodes Q and Qb to be 0 and 1, respectively The newly proposed CBS uses a clock branch sharing Scheme to sample the clock transitions, which efficiently reduces The number of clocked transistors and results in lower Power while maintaining a competitive speed.

A. CLOCK-GATING TECHNIQUES FOR LOW-POWER FLIP- FLOPS

Two novel low power flip-flops are presented in this project. Proposed flip-flops use new gating techniques that reduce power Dissipation by deactivating the clock signal and eliminate the clock duty cycle Double Gating in the following, apply gating technique not to the whole flip-flop, but separately to the master latch and to

the slave latch. Although, in this way, the introduced overhead is doubled[8], it will be shown that significant power dissipation reduction is obtained if input signal switching activity is low.

The second technique, named as NC2MOS Gating in the following, uses one only gating logic for the whole flip-flop. The gating logic is sequential with reduced overhead. Proposed gated flip-flops exhibit reduced minimum power dissipation and significant dependence of power dissipation with respect to flip-flop input pattern[5]. Proposed circuits have been designed up to the layout level in a 0.8µm 5V technology. For example, the NC2MOS Gated flip-flop provides 74% power dissipation reduction when input signal is idle. Main drawback of the proposed approach is the reduction of timing performances.
gating techniques. It then uses the covering relationship between the triggering transition.

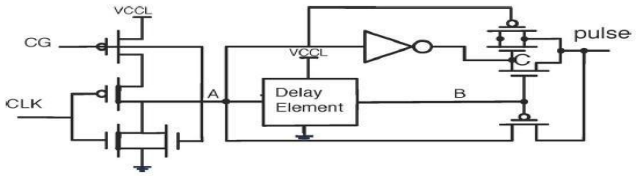


Figure 2 Pulse Generator Of DET-SRSFF

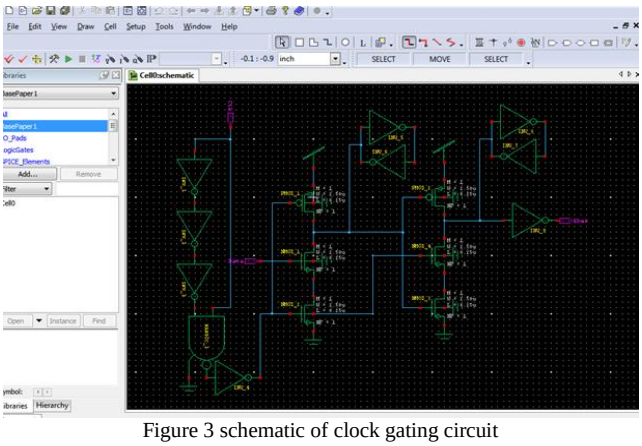


Figure 3 schematic of clock gating circuit

The figure 3 describes the schematic circuit of proposed clock gating technique which is used to avoid Asynchronous Behavior of the Internal Clock Signal by the condition of CLK ≠C. the switch T2 will stay OFF when CLK≠C , and C will synchronize with **CLK**. In the next half cycle where CLK =C , the switch T2 turns ON, but since they are equal, the flip-flop will not be triggered until C changes, which follows **CLK** when T2 is ON.

The pulse generation circuit which is provide clock generation for the entire circuit. The simulation result of Gating Circuit to avoid an asynchronous C shown in figure 4. When D changes while the **CLK** is 1, transistor T2, the one closer to **CLK**, will be turned OFF immediately, and C will remain the same. and the power obtained for the gating circuit as 1.297(mw) which is comparatively less than first gating circuit. when D = Q, since it would be unnecessary to sample the same signal value to store into the flip-flop. Transitions of D are used to assert the CG signal. The C is the internal clock pulse that triggers the flip-flop.

B. TIMING ANALYSIS

Parsing	0.01 seconds
Setup	0.05 seconds
DC operating point	0.00 seconds
Transient Analysis	0.14 seconds
Overhead	2.57 seconds
---	---
Total	2.77 seconds

Timestep and Integration options:
* relq|relchgtol = 0.0005

V. PROPOSED SHIFT REGISTER DESIGN RESULT ANALYSIS.

The figure 4 explained combined explicit and implicit design of sequential circuit design pulse width of is 140 ps, which is the required minimum width for a pulsed-latch at 0.75 V under the nominal process corner. The delay buffer that generates imposes a delay of 260 ps, so that the window for timing speculation is 400 ps wide. Extra delay buffers were inserted into all the circuits to fix hold violations.

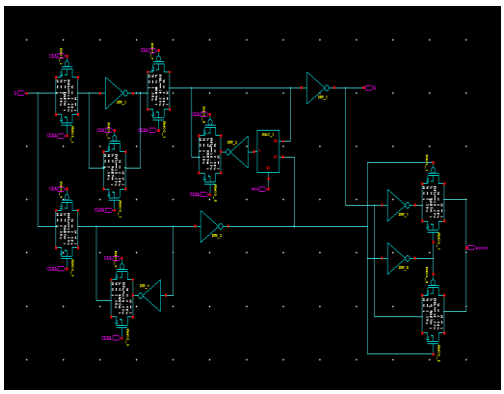


Figure 4 Edge Trigger Razor flip flop for timing issue Correction

The benefit from error-free mode increases rapidly as the number of timing errors occurs at the stage operating error-free mode. Fig.5.8 shows the relationship between overall timing penalty and the number of timing errors assuming that the timing errors continue to occur at a certain stage sequentially. Once an error occurs, our method does not have to pay the penalty for subsequent errors until error-free mode ends.

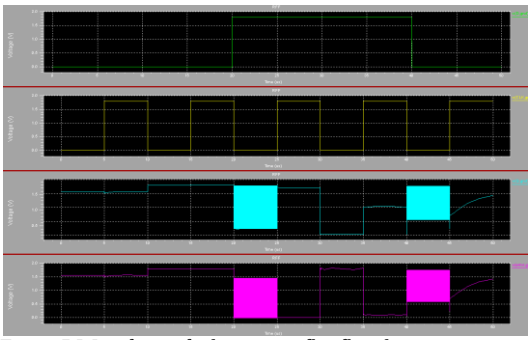
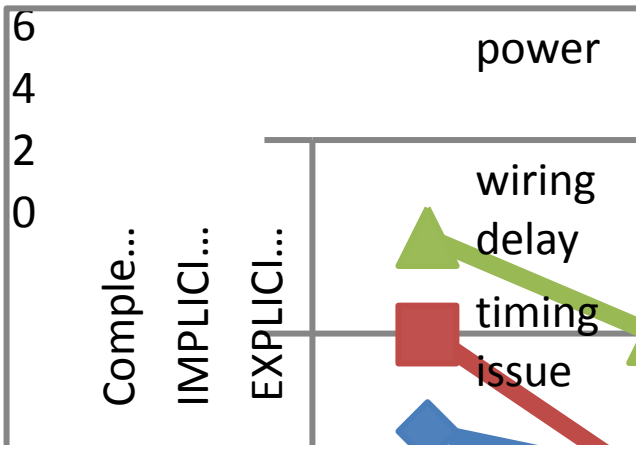


Figure 5 Waveform of edge trigger flip flop design



VI CONCLUSION

The design and analysis of Low-power and area-efficient shift register using pulsed latches are done successfully. The shift register reduces area and power consumption by substituting flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

Furthermore the design of edge trigger low area flip flop design for sequential circuits as well as clock generations circuit also discussed and designed, they are gives best case result of existing methods comparing area ,power and timing error.

REFERENCES

[1] *Analysis of Low-Power and Area-Efficient Shift Registers using Pulsed Latch* P. Rahul Reddy at al(2016),

[2] '*Content-Addressable Memory (CAM) Circuits and Architectures'* Kostas Pagiamtzis (2006)

[3] '*A Low-Power Ternary CAM With Positive-Feedback Match-Line Sense Amplifiers N*'. Mohan and M. (2009)

[4] '*A Mismatch-Dependent Power Allocation Technique for Match-Line Sensing in Content-Addressable Memories'* S. S. Chen, Z. H. Kong, (2011)

[5] '*Low-Leakage Storage Cells for Ternary Content Addressable Memories* N. Mohan and M. Sachdev,(2009)

[6] '*Match Sensing Using Match-Line Stability in Content-Addressable Memories (CAM)*'O. Tyshchenko (2008)

[7] *Hybrid-Type CAM Design for Both Power and Performance Efficiency* Yen-Jen Chang (2008)

[8] *Dual-Edge Triggered Storage Elements And Clocking Strategy For Low Power Systems* Xiaowen Wang, and William H. Robinson,

[9] "*A novel high speed sense amplifier based flip-flop* A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra.,2005