DESIGN OF A HIGH THROUGHPUT CMOS ADC USING HYBRID INCREMENTAL AND CYCLIC CONVERSION SCHEME

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***Abstract*-This paper describes the design of ADC architecture that is based upon hybrid scheme. The input voltage is supplied to the switches, to drive the operational transconductance amplifier, whose output is fed as an input to the comparator. The comparator used in this work is a dynamic latch comparator. An 8-bit counter is used to fetch the output. The schematic of 8-bits ADC is recognized through realization of the developed circuit at 180nm CMOS technology with supply voltage of 1.8 V. The INL and DNL are calculated, with resultant values -0.9/+1.4 and -0.8/+1.2. The proposed ADC is designed with an accuracy of eight-bits at sampling rate of 33.43 MHz. At 180nm technology, this incremental ADC has power dissipation of 1.975mW, calculated using Cadence virtuoso tool, and the results are verified in cadence layout editor.**

Keywords: **Hybrid scheme, dynamic latch comparator, counter, power dissipation, INL and DNL**.

1. INTRODUCTION

The hybrid scheme as the name suggests is combination of two different techniques used for analog-to-digital conversion. Hence, this scheme involves incremental and cyclic conversion scheme. The incremental method for data conversion basically operates on the principle of delta-sigma ADC, while cyclic method follows the principle of pipelined ADC. The hybrid scheme is more advantageous as; it has the capability to optimize the trade-off between resolution conversion and time conversion. The hardware for both incremental as well as cyclic scheme is shared, which leads to compact circuitry.

2. ORGANIZATION OF PAPER

This paper represents an analog-to-digital converter which is implemented using a hybrid incremental and cyclic conversion scheme [1], in order to achieve higher conversion rate while keeping the high precision features. The schematic is designed at a 180 nm technology. The input voltage of 1.8 V is supplied to the switches [2], to drive the operational transconductance amplifier [3], whose output is fed as an input to the comparator. The comparator used in this work is a dynamic latch comparator [4], which plays a vital of comparing the input voltage from the OTA to the reference voltage. The resultant output voltage from the comparator is given as an input to an 8-bit counter [5] that is used to fetch the output.

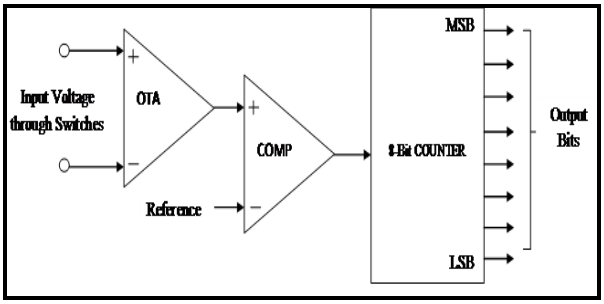

Fig. 1: Block Diagram of the ADC Architecture**.**

The block diagram for the hybrid scheme ADC is as shown in figure 1 in which, the input signal given is a voltage analog signal. Input is fed to the operational transconductance amplifier through the switches, the output of which is given as an input to the comparator circuit, whose function is to compare the given input value to the reference signal, now the resultant data is fetch by the counter, for the desired output bits.

3. CIRCUIT DESIGN

Low power and high speed conversion are the parameters that can be easily achieved by both incremental (delta-sigma) ADC and cyclic (flash) ADC. The whole circuit design is implemented through switched-capacitor technique.

3.1 SCHEMATIC OF HYBRID ADC

The design of hybrid ADC requires having an analog input signal of the supply voltage 1.8V, which is fed with the help of a CMOS switch. The schematic of the switch used is as shown in figure2.
In this circuit the NM0 is set at active “high”, while the PM0 is set at active “low”, for the switch to be in “ON” condition.

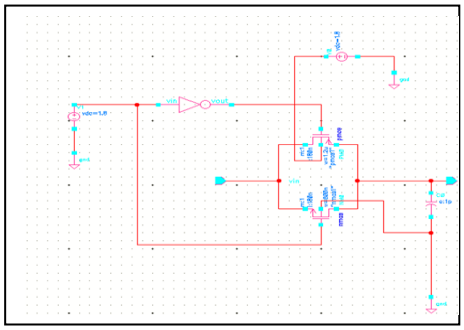

Fig.2: Schematic of a CMOS Switch.

The input signal is given at the port Vin. The resultant voltage at the Vout port is steered to the OTA.

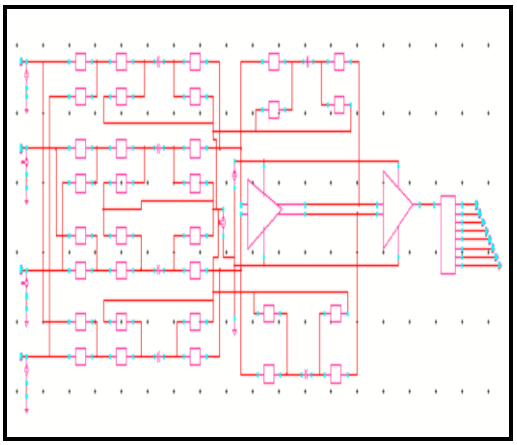

Fig. 3: Schematic of the ADC [6]

As the input is received by the OTA, it acting as a differential amplifier with CMFB block generates an input voltage for the following comparator by amplifying the difference of the voltage given to it.

3.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER:

The OTA has two operational phase, the sample and hold phase respectively. When the sample phase is in operation, the respective switches for the sampling are closed, while those assigned for the hold phase are kept open, and vice-versa. The schematic of OTA used in the ADC is as shown in figure 4. The folded cascode circuitry is used for the amplification of the input signal, with a following common source amplifier.

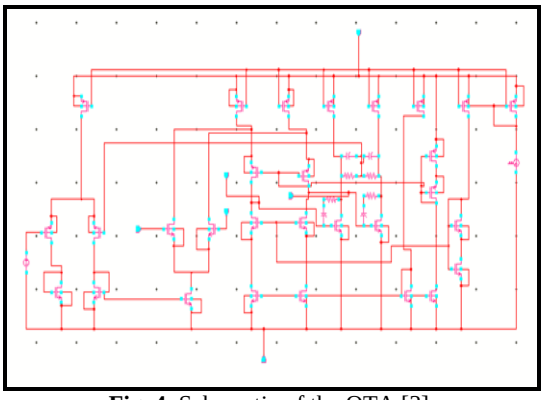

Fig. 4: Schematic of the OTA [3].

The NMOS differential pair is opted for the input stage, in order to attain higher transconductance. The folded cascode structure can realize higher gain when used with a common source amplifier M ~ M, as it reduces the overdrive voltage caused due to cascode structure.
The gain achieved of the OTA is 67.6dB, with a power dissipation of 44.02nW.

3.3 DYNAMIC LATCHED COMPARATOR

There are three different modules, which combine to form the dynamic latched comparator. The current mirror circuit followed by a flip-flop and then a latch are those vital modules. Two clocks are provided to the comparator circuit, which are represented as c1 and c2 respectively. The schematic of the dynamic latched comparator is as shown in figure 5.

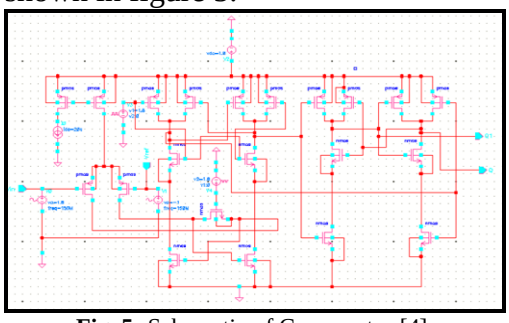

Fig. 5: Schematic of Comparator [4].

The two operating modes are: regenerating mode, and reset mode. The comparator is designed at 180nm technology, with a supply voltage of 1.8V, and sampling frequency of 225MHz to the input signal. The designed comparator exhibits the resolution of 8-bits.

3.4 EIGHT-BIT SYNCHRONOUS BINARY COUNTER:

A counter can be easily described as a device, whose sole purpose is to count (or store) the number of processes or event that takes place in certain interval, usually synchronized with a clock signal. The

binary counter can be implemented using variety of architectural arrangement. The counter shown in figure 6 is realized using eight synchronous D flip-flops.

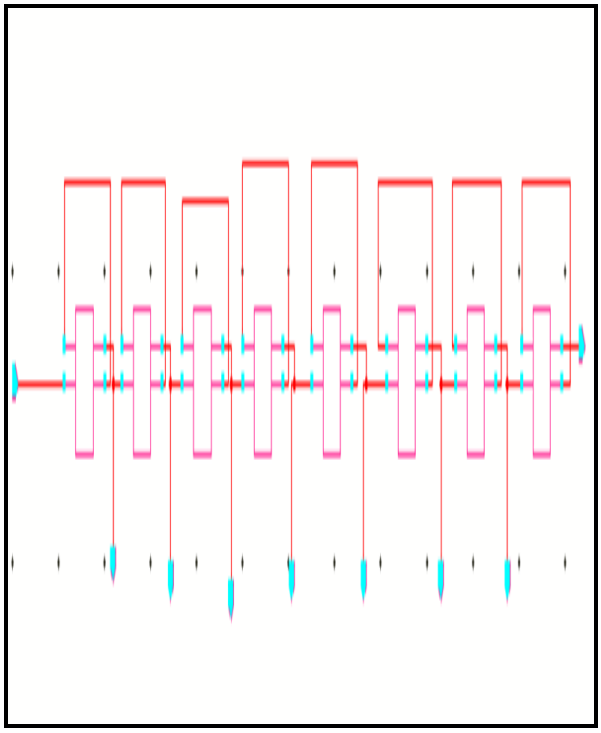

Fig. 6: Schematic of 8-Bit Synchronous Counter**.**

The designed counter is a synchronous up counter, which implies that the counter will efficiently count to eight bits and then it will reset again to the initial condition. The voltage range of the counter is from 0 to 1.8 volts.

4. EXPERIMENTAL RESULTS AND SIMULATIONS:

The two different ADCs are compared on the basis of their designing, simulations and schematics. The simulations are conceded on cadence tool, with 180nm design technology of present work and, the supply voltage of 1.8 volts.

Table 1: Design Specifications.

Parameters	Values
Technology	180 nm
Sampling Rate	33.43MHz
Power Supply	1.8V
Stop Time	600 ns
Resolution	8-Bits
Power	1.975mW
Reference Voltage	1.8V

The transient response of the ADC is as shown in figure 7, which is observed at a sampling rate of 33.43MHz for the resolution of 8-bits.

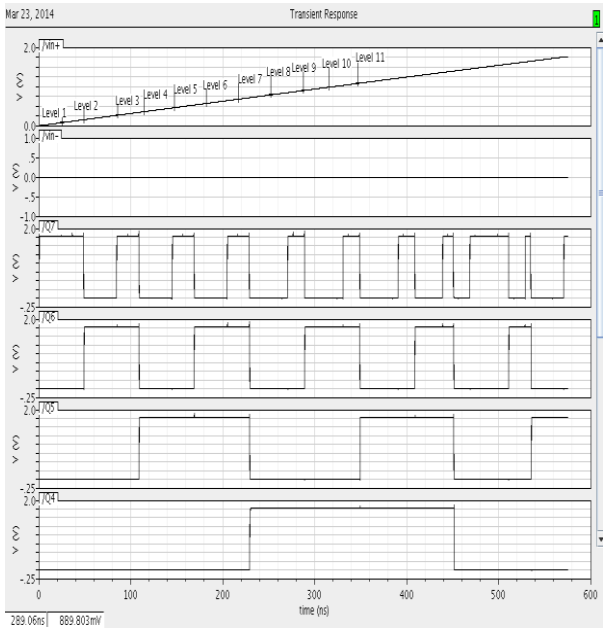

Fig. 7: Transient Response of Hybrid ADC.

The results are generated with the stop time of 600ns. The first bit (Q7) represents the MSB, and the last bit (Q0) represents the LSB of the output. The results are verified on the cadence layout editor. The layout of the designed hybrid ADC is as shown in figure 8. The results of the designed hybrid ADC are compared with ADC implemented using folding and interpolation architecture [8].

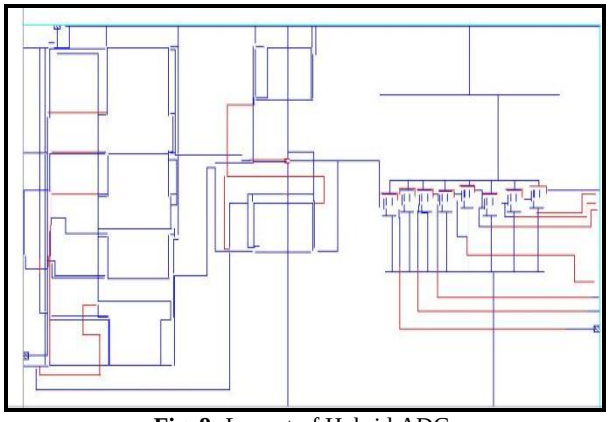

Fig. 8: Layout of Hybrid ADC.

Table 2 is a comparison table that shows the difference between two ADCs designed at 180 nm technology, with an increased sampling rate of 33.43MS/s, and resolution of 8 bits.

Table 2: Comparison between Folding Interpolation and Hybrid ADCs.

Parameters	**Previous Work [10]**	**Present Work**
Technology	180 nm	180 nm
Resolution	8-bits	8-bits
Power Supply	1.8 V	1.8 V
Power	18 mW	1.975 mW
Sampling Rate	30 MS/s	33.43 MS/s

5. CONCLUSIONS:

The hybrid ADC represented in this paper has a resolution of 8-bits, along with the power consumption of 1.975mW, at the sampling rate of 33.43 MS/s, when compared with previous work.

6. REFERENCES:

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