DESIGN OF ASYNCHRONOUS VITERBI DECODER USING 4-PHASE DUAL RAIL ENCODING: A TECHNICAL REVIEW

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Abstract*- Fordesigning any digital communication system power dissipation factor is the main concern. This review paper describes different decoding techniques used to design Viterbi decoder for low power consumption. It also describes various handshaking protocols used to make Viterbi decoder asynchronous and to communicate with various units of Viterbi decoder. It also state various parameters like bandwidth, speed, area overhead which is also helps to reduced power dissipation by calculating *or controlling it.

***Keywords*- Convolutional encoder, Viterbi Algorithm, Viterbi Decoder, Asynchronous, 4-Phase dual Rail, VHDL**

1. INTRODUCTION

In any digital communication System the transmission oferror free data with low power consumption as well as the system which consist small area is the main concern and these are the main issues in mobile communication and in wireless communication. In mobile communication system, the Viterbi decoder occupies greater chip area which directly related to the power loss. Therefore, the implementation of a low power Viterbi decoder is necessary.

Viterbi algorithm is a widely used scheme for decoding convolutional codes in communication system. The Viterbi Algorithm is developed by An American electrical Engineer Andrew James Viterbi in 1967. It performs Maximum Likelihood decoding by reducing its complexity. ML decoding calculates the hamming distance for each path and then estimate the total number of path and which have the smallest hamming distance message sequence transmitted through that path. Therefore it's very Complex process for finding the correct path. The Viterbi Decoder solves this problem without estimating entire trellis. Trellis provides a good background for understanding decoding.

II. TECHNICAL REVIEW

[1]This paper proposed an asynchronous architecture of FPGA to decrease the power dissipation. They mainly concentrated on switch block and clock distribution of FPGA to reduce the power feeding.

[2]This paper presents an asynchronous adaptive priority round robin arbiter.To make the system an asynchronous 4-phase dual rail encoding is used. This protocol is used to overcome the problem of area overhead and for accurate bandwidth purpose. It works in four steps request, acknowledge, clear request, clear acknowledge.In the result the speed is improved by 18%-50.4%.

[3] This paper described an asynchronous Viterbi decoder in which hybrid register exchange method is used. HREM is the mixture of trace back method (TBM) and register exchange method. It overcomes the problem of switching activity which introduces in TBM and REM. The constraint length of the convolutional encoder is K= 3 and code rate r=1/2. An asynchronous circuit have number of blocks that communicate with each other by using handshaking protocol. Simulation results for Asynchronous system and power analysis is described. The resultant dynamic power consumption is 1mw which is proposed and it is less than the 1.28mw reference power consumption.

[4] In this paper an asynchronous FPGA architecture for low power consumption is proposed. Conventional logic block consumes more dynamic power. Due to this, when information is recognizing in incorrect timing the power dissipation is more. To overcome this problem data arrival detector architecture is proposed.

[5]This paper described the techniques by using the power consumption can be reduced. Registers are used to store the survivor memory. To achieve low power consumption, the one important parameter is added to the minimum transition and exchangeless algorithm, threshold. To design convolutional encoder the required parameters consider as k=5, r=1/3, m=4. Results are accomplished as such with total 75% power consumption by designing the Viterbi decoder with 0.15um technology.

[6] This paper based on review of Viterbi decoder for trellis coded modulation system. It uses in application like space communication, geostationary satellite communication network. The code rate of convolutional encoder is ¾ and the shift register is 6 which known as constraint length. The design steps are described to design Viterbi algorithm which works in three stages they are BMU, ACSU and storage shortest path known as survivor path.

[7]This Paper described the different decoding techniques for reducing the switching activity by evading the unnecessary memory operations. It also discuss the comparative study of synchronous and asynchronous Viterbi decoder by mainly focusing on low power consumption. After examining literature survey, in their proposed work they will use different power reduction technique like 4- phase bundle data protocol, pipelined architecture, opaque latches and Minimum Transition Hybrid Register Exchange method as a decoding method as it reduces switching activity to achieve less power consumption.

[8]In this paper, new decoding scheme for Asynchronous Viterbi Decoder using Hybrid Register Exchange Method is proposed.This method uses Dual rail protocol for convertingHREM system into asynchronous system by using clock AND-ing operation.From simulation results the dynamic power is reduced to 0.12mW for single clock.

III CONCLUSION

From the literature survey it is observed that using different methods Asynchronous Viterbi decoder has been designed.For designing an asynchronous Viterbi decoder for low power consumption number of handshake protocols has been used. Due to unnecessary memory operations switching activity is more, to overcome these problem this paper describes various decoding methods. It also states the various handshake protocols which is helpful in designing Asynchronous Viterbi decoder. By calculating or controlling various parameters like bandwidth, speed, area overhead, energy consumption (static as well as dynamic) power reduction can be achieved.

In Viterbi decoder ACS unit and SMU unit consumes more power. While designing the Viterbi decoder it should be taken into consideration. To make the system asynchronous we will use 4-phase dual rail protocol as a handshake protocol.

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