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A POWER GATED FAST AND WIDE RANGE LEVEL SHIFTER

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***ABSTRACT*- In an MSVD system, level shifters (LSs) are required on the boundaries between the circuit subsections operating at different power supply voltages to up-convert signals from the VDDL to the VDDH voltage level. In this brief, a new LS is presented for fast and wide range voltage conversion. Because of a novel architecture combined with the use of multi-threshold CMOS technique, the proposed circuit guarantees robust voltage shifting from the deep sub-threshold to the above-threshold domain while exhibiting fast response and low energy consumption. We also propose a level shifter uses analog circuit techniques and standard zero-Vt NMOS transistor without adding extra mask or process step. No static power consumption and stable duty ratio make this level shifter suitable for wide I/O interface voltage applications in ultra deep sub-micron.**

I INTRODUCTION

ENERGY efficiency is one of the most important issues to address in today's System on-a-Chip designs. Among the techniques known in the literature to reduce power consumption, those based on power supply voltage reduction are considered very effective even though they can severely penalize speed performances [13].

Ultra-low energy digital complementary metal–oxide–semiconductor (CMOS) circuits are rapidly gaining a wide interest due to the large proliferation of battery-powered electronic devices [1]. Power supply voltage (V_{dd}) scaling below the transistor threshold voltage (V_{th}) is one of the most effective approaches to achieve low-energy consumption. However, energy saving is obtained at the expense of reduced computational speed and increased sensitivity to temperature and process variations. While acceptable for niche markets, such as wristwatches and hearing aids, the delay penalty can be very limitative for a broader set of applications [7].

Sub threshold operation provides the lowest energy per operation when compared to traditional higher supply voltages [3,5,7,13] for applications in both general and reconfigurable electronics. However, this increased energy efficiency comes at the price of a substantial degradation of performance. By extending the concept to voltage island methodologies, which have become widely adapted in recent years, circuits can benefit from the low power aspects of sub-threshold operation by running the vast majority of the non-critical circuits at lower voltage than the high performance circuits – particularly for reconfigurable circuits which include peripheral circuits requiring higher supply voltages (i.e. SRAMs, configuration logic, IO, etc).
Numerous design techniques have been proposed to reduce standby leakage in digital circuits. Out of this rich set of solutions, power gating has proven to be a very effective approach to minimize stand by leakage while keeping high speed in the active mode. It is based on the principle of adding devices, called *sleep transistors* The most common implementation of Multi Threshold Complementary Metal–Oxide–Semiconductor (MTCMOS) for reducing power makes use of sleep transistors. Logic is supplied by a virtual power rail. Low V_{th} devices are used in the logic where fast switching speed is important. High V_{th} devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode. High V_{th} devices are used as sleep transistors to reduce static leakage power [3,5,13].

In this brief, a new LS is presented for fast and wide range voltage conversion. Because of a novel architecture combined with the use of multi-threshold CMOS technique, the proposed circuit guarantees robust voltage shifting from the deep sub-threshold to the above-threshold domain while exhibiting fast response and low energy consumption. We also propose a level shifter uses analog circuit techniques and standard zero-Vt NMOS transistor without adding extra mask or process step. No static power consumption and stable duty ratio make this level shifter suitable for

wide I/O interface voltage applications in ultra deep sub-micron.

The rest of this brief introduces the novel level shifter with the sleep transistor by reducing leakage and the power. Next the related works and the Voltage Conversion in Multi supply Voltage Designs are considered in Section II. Then, in Section III, the proposed is presented. Section IV presents a experimental Results and performance analysis to illustrate the effectiveness of the approach. Finally, the conclusions are summarized in Section V.

II RELATED WORKS AND THE VOLTAGE CONVERSION IN MULTISUPPLY VOLTAGE DESIGN

Low-power design methodologies range from the device/process level to the algorithmic level. Of all these techniques, lowering the supply voltage (V_{DD}) is the one that significantly reduces the power consumption because of the quadratic relationship between the supply voltage and the dynamic power consumption. To compensate for the performance loss due to a lower supply voltage, a transistor's threshold voltage (V_T) should also be reduced. However, this causes an exponential increase in the sub-threshold leakage current. Therefore, an important research area today is to develop circuit techniques to reduce the sub-threshold leakage currents that are caused by the reduced V_T .

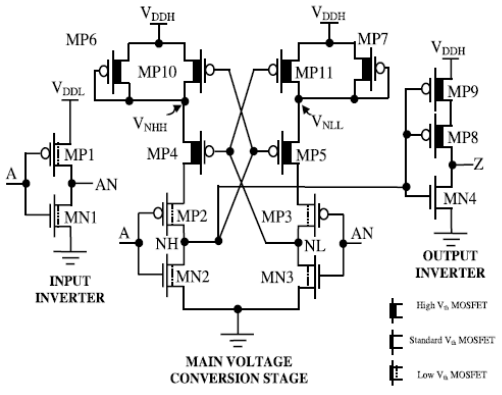

Fig.1 LS design

The LS circuit is shown in Figure. It combines the multi-threshold CMOS design technique along with novel topological strategies. The circuit consists of an input inverter, a main voltage conversion stage and an output inverting buffer. The input inverter (MP1/MN1) is designed using low threshold voltage (lvt) transistors. This provides fast differential low-voltage input signals to the main voltage conversion stage. To have higher strength of the pull-down network, also MN2 and MN3 are lvt transistors. Then, two lvt pMOS devices (MP2 and MP3) are added to both the branches of the circuit.

These devices limit the cross-bar current that is the current flowing in the pull-up network and opposing to the discharge of NH (or NL) node at the beginning of their high to low transition. To further facilitate the high to low transition at the nodes NH and NL, MP4 and MP5 are high threshold voltage (hvt) transistors. This choice also reduces leakage current flowing through the pull-up networks when MP4 or MP5 are turned off. However, using hvt, pMOS transistors has the counter effect of slowing the low to high transition of the nodes NH and NL. Therefore, to reduce the switching delay, a pull up network able to self-adapt its strength to the actually occurring transition would be desirable. This behavior was obtained by introducing the parallel connected hvt devices MP6-MP10 and MP7-MP11, with MP6 and MP7 being diode connected transistors[6]. The latter devices impose two variable virtual power supplies *V*NHH and *V*NLL on the two branches of the circuit. Therefore, the strength of pull-up networks is adapted to the next output switching transition. That is, assuming that the output Z is initially low (high), the pull-up network of the left branch is weakened (strengthened) and that of the right branch is strengthened (weakened), thus speeding-up a low-to-high (high-to-low) output transition. The introduction of hvt MP10 and MP11 devices controlled by NH and NL voltages represents a significant difference with respect to the circuit previously proposed in [13].

Figure shows the behavior of this LS with reference to a low to high input signal transition. Before the rising (falling) transition of the input

signal A (AN), the nodes NH and NL are held high and low, respectively. Therefore, MP10 is switched off and MP11 is switched on. Thus, the left branch of the circuit is power supplied at VDDH-*V*dsat,MP6, whereas the right one is power supplied at the full VDDH voltage. As the input signal switches, the transistor MN2 is turned on and the node NH starts to be discharged.

This process (phase 1) is favored by the initial supply voltage level NHH, which reduces the source to gate voltage of MP4 and, due to the body effect, increases its threshold voltage. Owing to this, MP4 is weakened, thus speeding up the discharge of the node NH. In the meantime, the stronger pull-up of the right branch charges the node NL and a positive feedback is triggered causing MP4 to be turned off (phase 2). This allows the discharging of NH to be further accelerated. A LS suitable for robust logic voltage shifting from near/sub-threshold to above threshold domain has been presented. This circuit exploits proper design strategies to increase the operating speed while maintaining very low energy consumption and large voltage conversion range. When used to up-convert voltage signals from the deep sub-threshold regime, the design outperforms all the previous LSs.

III PROPOSED LS DESIGN

Fig.2. shows a novel low to high level-shifter which operate in ultra low core voltage(0.6V) and wide I/O voltage ranges(1.65V~3.6V) with small duty ratio variation under process, voltage and temperature corners. Thin gate-oxide input stage of level shifting block is used to operate under ultra low core voltage. To avoid source drain over stress voltage for MN11 and MN12, Thick gate-oxide zero-Vt. Transistor MN31 and MN32 is used. In case of input signal, A, changes high to low, when A is high MN11 is 'off' and MN12 is 'on' at that time the MP11 and MP12 is 'off' due to gate voltage MP11 and MP is below those transistor's threshold voltage. Even MN31 is 'on' during this event leakage current does not exist due to MN11 and MP11 is 'off'.

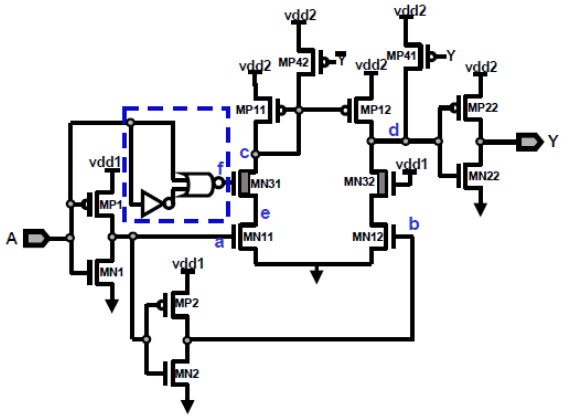

Fig.2 Proposed LS Design

When A switches to low, MN11 is turn 'on' which makes MP12 'on' and MN12 'off'. MP12 makes the final level-shifter output voltage to low. Switch element turns on MN31 only A transfer low to high. After finishing logic transition, MN31 is 'off' and cuts the leakage path without feedback path which was used conventional Type-II level shifter. At that time the gate voltage of MP11 and MP12 is discharged through the MP11 which makes MP11 and MP12 is 'off'. In this case both MN12 and MP12 is 'off' temporary. If those transistors are off at the same time input node-d is floating. To prevent this event MP41 and MP42 are added.

IV EXPERIMENTAL RESULTS

The proposed level shifter circuits with sleep transistor are simulated by using TINA. The experimental results are given in Table 1 and the simulation results of layout and the waveforms are shown in the fig.3 and fig.4.

S.no	Parameter	Existing	proposed
1	Power	1u	100n

Table 1: Experimental result

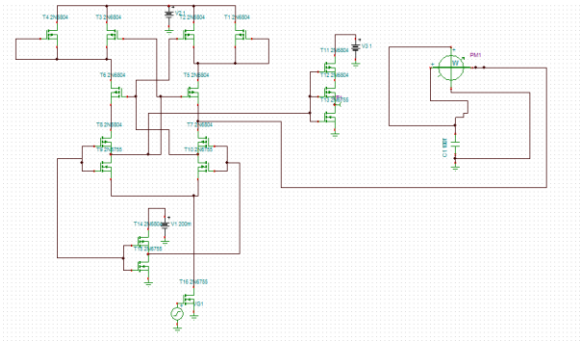

Fig.3 proposed layout

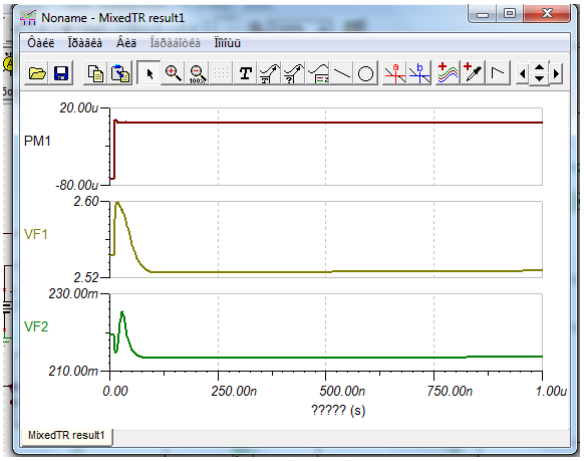

Fig.4 Waveform of proposed layout

V CONCLUSION

In this brief, a new LS is presented for fast and wide range voltage conversion. Because of a novel architecture combined with the use of multi-threshold CMOS technique, the proposed circuit guarantees robust voltage shifting from the deep sub-threshold to the above-threshold domain while exhibiting fast response and low energy consumption. We also propose a level shifter uses analog circuit techniques and standard zero-Vt NMOS transistor without adding extra mask or process step. No static power consumption and stable duty ratio make this level shifter suitable for wide I/O interface voltage applications in ultra deep sub-micron.

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