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Topologies of SRAM: A Review

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***Abstract*- We are evident of advancement of process technologies in semiconductor industry, which has offered us, increased performance of integrated circuits, improves the speed, power dissipation, size and reliability. To maintain, this pace in the semiconductor industry, it is necessary to overcome associated challenges of technology scaling. Memory, being a major part of any system, is also evolved by the time, plays an important role to improve the performance of the System-on-chip (SoC) products. This paper gives a systematic and comprehensive insight to build an understanding SRAM bit cell circuit, architectures, designs and analysis techniques.**

***KEYWORDS* – Static Random Access Memory (SRAM), Cache, Bit Line, Transmission Gate (TG), Bit Cell, Low Swing.**

1. INTRODUCTION

Since 1965, it is the Moor's law, scaling the technology and in results, the performance of VLSI designs is reached at the level of the five orders of magnitude in the last four decades [1]. Moore's law, states that the doubling of the number of transistors per generation on an integrated circuit almost every 2 years (usually 18–24 months) [2]. In the present time, The semiconductor industry, is still trying to match the speed of scaling the technology according to the Moor's Law, and it is only due to shrieked transistors and by the overcoming the limitation of technology scaling. He also estimated that the scaled technology for microprocessors would also reduce the manufacturing cost per function, exponentially for future generation technology.

Generally, scaling the minimum feature size, length and width by about 30% (Moore's magic number) for each new technology generation, theoretically gives the following:

1. Doubling of device density and lowering of area by (0.7*Y×0.7*X) ~ 50%, helps packing of more devices in the same area, which effectively reduces the cost per transistor;
2. Reduces the total capacitance by 30% which allow gate delays to decrease by 30%, resulting in increase in operating speed up to 43%;
3. Accordingly the power consumption (*Power* $\propto CV^2 f$) should decrease for a given circuit by 30–65% due to smaller transistors and lower supply voltage [3].

Similarly, all other technology generations have been derived. Scaling of supply voltage drastically reduces the dynamic power by the relation of quadratic between supply voltage and static power. While lowering of V_{DD} increases delay, therefore, the device threshold voltage (V_{TH}), must also decrease in order to maintain the drive current. Lowering V_{TH} leads to an exponential increase in leakage power.

Moreover, scaling for minimum feature size and closely matched devices also play a significant role while when designing Static Random Access Memories (SRAMs), therefore, they are the first to suffer from the exponential trends of scaling. The continued scaling of CMOS technology has yielded several problems like process induced variations, soft errors, degradation of transistors due to ageing etc. However, these problems were not much serious in the earlier generations.

2. STATIC RANDOM ACCESS MEMORY (SRAM)

The first commercialized MOSFET based memory came into existence in seventies. In 1968 [4], Robert Dennard explained the concept of dynamic memory cell with a single MOSFET and a capacitor at IBM and successively, MOSFET based dynamic random access memory (DRAM) chip with 2k-bits came into existence with controlled leakage current in 1971. However, performance of DRAM has not matched the pace with the performance of the processors because of long access time and due to requirement of more power and there is also requirement to refresh periodically for use data without lose in memory cells [5,6].

To fill this growing gap between the performance of processors and DRAM created the hierarchy of different levels in the processor architectures. It results, memory hierarchy range from faster, small sized and expensive on chip memories to slower, large sized and inexpensive memories like DRAM memories. To match the performance requirement, a processor fetches the most frequently used data and instruction from the closest memory to itself, known as "cache" memory. These are also labeled as L1, L2 and even L3, which are static random access memories (SRAMs) [1].

Although, SRAMs dominate in performance but SRAMs of high capacity cannot be embedded, due to area limitation on chip and the high cost per bit. Latest trends shows that the percentage of embedded SRAM in System-on-Chip (SoC) products will increase further from the current 84% to as high as 94% by the year 2014 [7]. Moreover, there is a huge demand of cache memory in modern computer systems as microprocessors design has been shifted to multi-core architectures and the share of SRAM on a die has drastically increased from 20% in 1999 to 94% in 2014 [1].

This growing trend is mainly to provide faster access by eliminating the delay across the chip interface. Also embedded memories are designed with rules more aggressive than the rest of the logic on a SoC die, therefore, they have dense packing which makes them more prone to manufacturing defects. This trend has mainly grown due to ever increased demand of performance and higher memory bandwidth requirement to minimize the latency, therefore, larger L1, L2 and even L3 caches are being integrated on-die. Hence, it may not be an exaggeration to say that the SRAM is a good technology representative and a powerful workhorse for the realization of modern SoC applications and high performance processors. In addition, SRAM scaling signifies the huge potential of decreasing the cost per function in microprocessors as well.

3. ARCHITECTURE OF MEMORY

An SRAM is an array of cells and any cell can be accessed for read and write purpose with the help of addresses decoded by decoder, so called as Static Random Accesses Memory.

The basic architecture of the SRAM contains one or more rectangular arrays of memory cells with control circuitry to decode addresses for few basic and special operations. Since, the use of mobile, hand held and battery operated device with high data transfer rates, so memory densities are also increasing on these devices. So, SRAM makes up a large part of the system, which has requirement of the power and space on the system. Memories are also only responsible for almost half of the total CPU dissipation.

Therefore reduction of power and delay in memories becomes an important issue. In this case, it is require finding out the total power consumption by the system and delaying in the different blocks as well as cells of memory to reduce the power consumption and delay. In the past, various semiconductor engineers have come with power efficient designs for on chip memories, allowing for better overall performance of the system. They reduced power consumption by adopting suitable techniques, such as circuit partitioning, increasing gate oxide thickness in non-critical paths, reducing V_{th} (dual V_{th}) etc. These technologies, like circuit partitioning technique had improved the speed of memories. The control block, the decoders and IO blocks are all in low V_{th}, whereas the memory cells, along with the sense amplifier are in high V_{th} [4]. But, a lot can be done to improve the speed, reduce the power consumption and delay.

4. ARCHITECTURE OF SRAM BIT CELL

Conventional 6T SRAM bit cell topology as shown in figure 1, is the widely used bit cell for cache memory in high performance microprocessor and on chip caches in SOCs. There are several topologies have been developed with the aim of different objectives like minimum bit cell area, low static and dynamic power dissipation, improved performance and better parametric results in terms of Static-Noise-Margin (SNM) and Write-Ability-Margin (WAM).

Other techniques like boosting the supply voltage, read and write assist circuitries in SRAMs have also

been proposed to achieve more stable data retention during read operations [8,9]. The main concern in SRAM bit cell design is a trade-off among these design metrics. For example, in sub-threshold SRAMs, noise margin (robustness) is the key design parameter and not speed [10,11]. Therefore, on the basis of their robustness these bit cell topologies are broadly divided into two categories: (1) non-isolated read port SRAM bit cell topologies (less robust), and (2) isolated read-port SRAM bit cell topologies (highly robust).

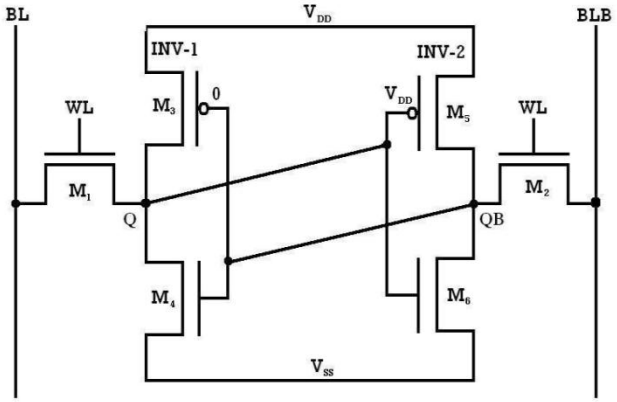

Figure 1. Conventional 6 T SRAM Bit Cell

4.1.1 Non-isolated Read-Port SRAM Bit cell Topologies

This is a less robust topology due to its poor read SNM. It happens due to the use of same pass –gate device for both read and write operations means there is no isolation between read and write ports. The tuning of the bit cell ratio is involved in this arrangement to achieve the read and write operation simultaneously. For both the operations properly sized device is required. Various developments in this category are as follows:

4.1.2. Five-Transistor (5T) SRAM Bit cell Topology

It is a high density low leakage current five transistor (5T) SRAM bit cell [12] as shown in figure 2, which has only one bit line to perform read and write operations via a single pass-gate device M1, . Writing into 5T bit cell enables by connecting the bit line to V_{DD} or V_{SS} respectively, when the word line is high or connected to V_{DD}. But correct sizing of the transistors is required to ensure sufficient WAM and read- SNM. Though, this design takes 15-21% less area for different processes, lower bit line leakage to 75%, and has a comparable read/ write performance to standard 6T bit cell but it has poor static noise margin and require a on-chip DC-DC to generate a pre-charge voltage of bit line. In 5 T SRAM bit cell read operation requires a pre-charge voltage (VPC) for read operation where V_{SS} <VPC < V_{DD}. While in the standard 6T SRAM pre-charged at V_{DD} before a read and write operation. Therefore, a possible bit line pre-charge voltage VPC levels for 5T SRAM bit is observed 340–860mV for worst case. A VPC of 600mV has been reported as the bit line pre-charge voltage level for a 0.18 μm CMOS Technology [1].

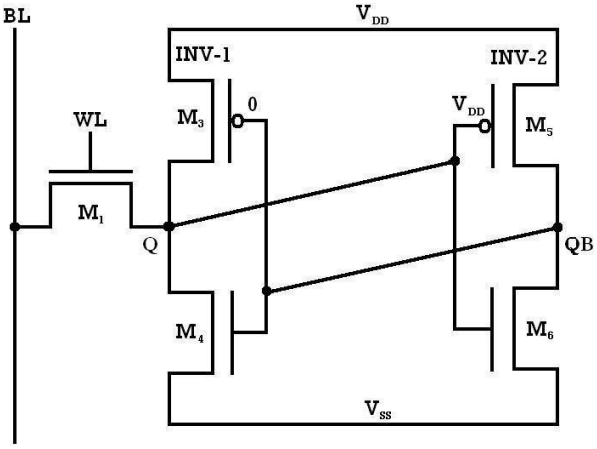

Figure 2. Five-Transistor (5T) SRAM Bit cell Topology

4.1.3. Transmission Gate Based Six-Transistor (6T) SRAM Bit cell

In the design of Transmission Gate based 6T SRAM bit cell [13], accessing and transferring of data can be accomplished by a transmission gate (TG) during the execution of read and write cycle through a single ended bit line or data line. There is a disadvantage of this TG is that it conducts perfectly for '0' as well as '1'in both direction, means, a read cycle can easily change the content of bit cell, due to the straight intervention of read current to the data storage node Q, as shown in figure 3. Thus the application of TG reduces the read SNM, ever beyond the 6T SRAM bit cell for an iso-area topology. In TG 6 T bit cell, to outline the benefits of technology scaling, all devices should be sized too large to achieve authentic read SNM. It is suggested to make the bit cell size more than twice

the convention 6T SRAM bit cell. Sharing of a header and footer per column enables the writing ability of the bit cell. However, it affects the stability of the other (non-accessed) bit cells, which are connected to the same bit line at the time of write cycle.

Because at the onset of a write cycle (when signal *wr_en* is activated), the footer will slow down the re-generative action of all the bit cells (or cross-coupled inverters) those sharing the same column for improving the write-ability of an accessed bitcell. The measurement results from a 2 Kb SRAM test-chip fabricated in 0.13 m bulk CMOS show a 64% energy saving as compared to a multiplexor (MUX) based memory [10]. While this bitcell topology takes more than 42% of area overhead as compared to standard 6T bit cell and fails to operate below 720mV but it manages to operate at sub-200mV V*DD*. Another major drawback with this design is that the increased leakage current from the bit line (BL) limits the number of bitcells per bitline to 16 [1].

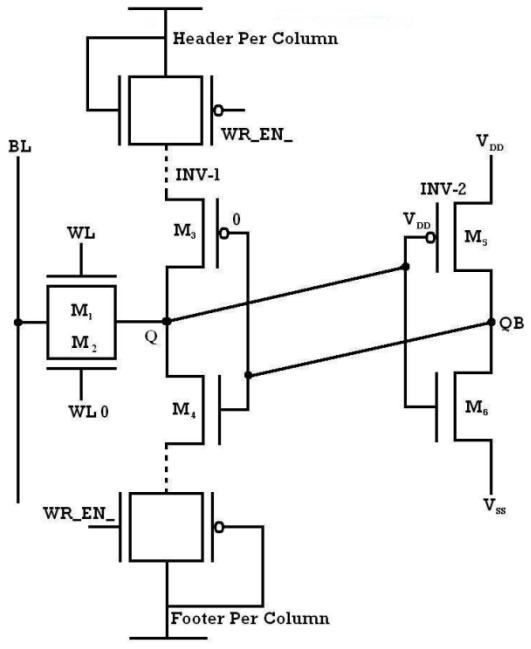

Figure 3. Transmission Gate Based Six-Transistor (6T) SRAM Bit cell

4.1.4. Ten-Transistor (10T) Schmitt Trigger SRAM Bitcell

The basic unit of this robust bit cell is an inverter pair and the characteristic of this inverter pair of the bit cell is improved with the help of modified configuration of Schmitt trigger as shown in figure 4 [14]. According to the modification in the direction of the input transition, it either increases or decreases the switching threshold voltage of an inverter which increases the read and hold SNMs effectively. It yields better read stability and write ability for sub-threshold operations at the cost of almost double area overhead than conventional 6T bit cell with 1.56 x and 2.3 x at V_{DD} of 0.4 V as compare to conventional 6 T SRAM respectively. It is more power saving at lower $V_{DD,}$ it is 18% and 50% in leakage and dynamic power respectively at 130 nm [1].

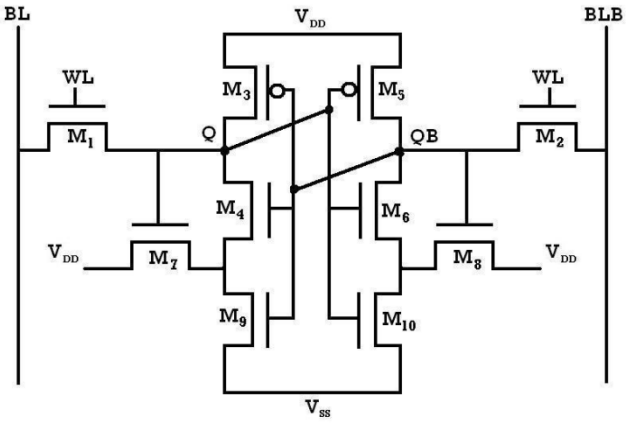

Figure 4. Ten-Transistor (10T) Schmitt Trigger SRAM Bitcell

4.2. Isolated Read-Port SRAM Bitcell Topologies

It is the topology, which has got a lot of attraction for lower supply voltage V_{DD} or sub-threshold operation [15, 16, 17, 18, 19, 20, 21, 22, and 10]. Reduction in supply voltage V_{DD} drastically reduces the SRAM bit cell noise margins and increases susceptibility to process variation. Therefore, to improve the poor noise margins or process variability at lower voltages, researchers moves towards the eight transistor (8T) or ten-transistor (10T) register file (1-read/1-write) type of bit cells than conventional six-transistor (6T). Though, it provides separate read port at the cost of extra silicon overhead and also limits the scope of scaling of future generation. Furthermore, with the optimized device size, a read-SNM free SRAM bit

cell can be aimed. The recent development of isolated read-port are as follows:

4.2.1. Eight-Transistor (8T) SRAM Bit cell Topology

This topology also known as a register file type of SRAM bit cell topology. It is an extension of standard 6T SRAM bit cell. It consists of separate read and writes ports for read SNM free bit cell [16, 18, 20, 21, 22]. In this topology, two transistors M7 and M8 are used to de couple the read and write operations. Here, Separate read (RWL) and write (WWL) word lines are used to control the read and write ports respectively for accesses the data of bit cell during the read and write operation. De-coupling of these two operations gives SNM-free read stability and overcomes the independency between stability and read current. But dependency between density and read-current is still there. This read port also introduces an additional leakage current path which was not in conventional 6T bit cell. Due to large area overhead and leakage power limited the application of this bit cell in comparison of conventional 6T bit cell because leakage power is the critical parameter of a SRAM design, particular for highly energy constrained applications.

This bit cell does not introduce read bit line (RBL) leakage current. In [22] the bit line leakage current from the un-accessed bit cells is managed by adding a buffer-footer, shared by the all bit cells in that word.

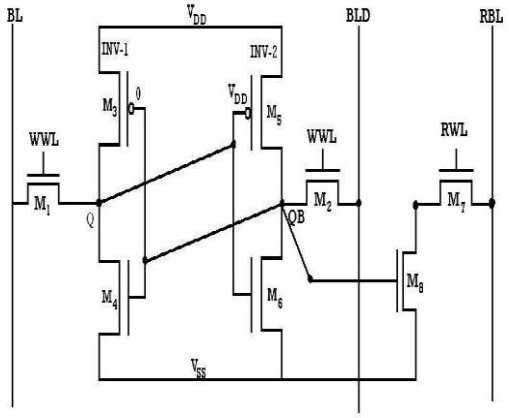

Figure 5. Eight-Transistor (8T) SRAM Bit cell Topology

4.2.2. Nine-Transistor (9T) SRAM Bit cell Topology

This bit cell topology contains three extra transistors along with conventional 6T bit cell which bypass read current from the data storage nodes and yields nine transistor (9T) SRAM bit cell as shown in figure 6 [19]. It makes a non-destructive read operation or SNM-free read stability. Although, it covers 38% more area overhead but have the read SNM of 9T SRAM bit cell for 65 nm is approximately 2 x better than the conventional 6T SRAM bit cell [1] and assures 23% better leakage power. Due to complex layout, thin cell layout structure does not suit in this design and presents jogs in the poly.

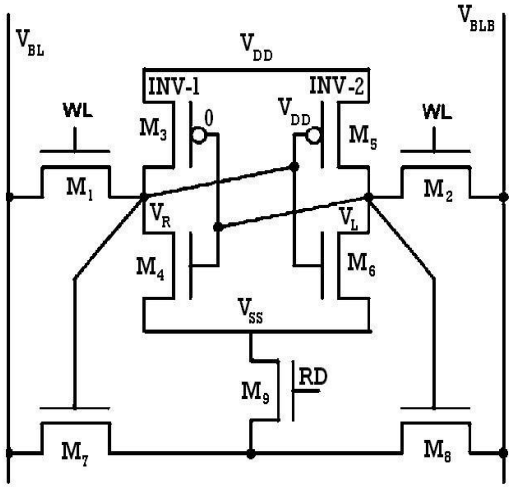

Figure 6. Nine-Transistor (9T) SRAM Bit cell Topology

4.2.3. Ten-Transistor (10T) SRAM Bit cell Topology

10 T SRAM bit cell has a separate read port of 4 transistors along with 6T SRAM bit cell [23] as shown in figure 7. Its write access mechanism and basic data storage unit are same as in conventional 6T bit cell. It shows the same advantages as the 8T bit cell, such as a non destructive read operation and ability to operate at ultra low voltages. But the problem of read bit line leakage current degrades the performance for read data correctly.

Specifically, the problem of the isolated read-port 8T cell is similar to that of the standard (non-isolated read-port) 6T bit cell. The data stored in the un-accessed bit cell gives a leakage current. This current goes through the same read bit line and

affects the same node as the read bit line from accessed bit line.

As a result, the leakage current from the all of the un-accessed bit cells, can pull-down RBL even if the accessed bit cell based on its stored data should not do so. This problem is known as an erroneous read. There are two additional transistors to improve the erroneous read by cutting off the path of RBL when RWL is low and yields a robust bit cell which is independent of the data stored. It shows better performance at lower V_{DD}.

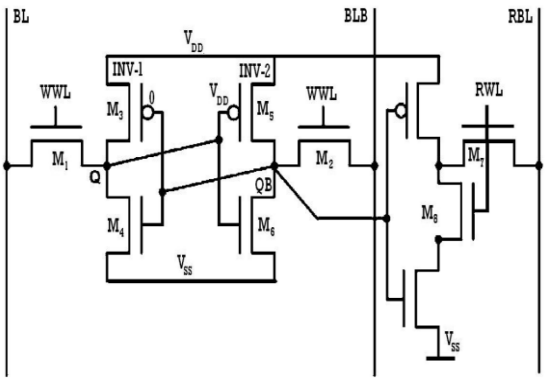

Figure 7. Ten-Transistor (10T) SRAM Bit cell Topology

IV. CONCLUSION

To match the pace of performance of different processors and System-on-Chip (SoC) products has given the pavement of innovation in this area. It is shown from the study of different SRAM bit cell that the isolated read port SRAM bit cells have improved read stability and process variation tolerance than non-isolated read port SRAM bit cell. But complex layout and extra silicon area overhead of isolated read port SRAM bit cell are the critical limitation of these designs. The implication of scaling of technology affects the stability and noise margins of standard SRAM design which motivated the semiconductor engineers to explore the alternative design for future technology generations.

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