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Design Analysis of XOR Gates Using CMOS & Pass Transistor Logic

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***Abstract*-This paper compares two different logic styles based on 45 nm technology for implementing logic gates of upto two inputs in terms of their layout area, delay and power dissipation. The XOR gate has been implemented & designed using CMOS & Pass Transistor logic on 45 nm technology .The schematic of proposed gate has been designed & simulated by using DSCH3& its equivalent layout has been developed &analysed using micro wind software. The result of computation shows that pass transistor logic can provide very high speed but in terms of area CMOS technology is superior to pass transistor based design.**

***Keywords*- XOR logic gate, 45nm technology, CMOS & pass transistor logic.**

I. INTRODUCTION

Active power and passive power are two major parameters for performance analysis of a device, active power is proportional to V_{dd}^2 and leakage power is proportional to V_{dd}, therefore ultra-low power logic circuits can be achieved by simply reducing power supply voltage (V). A lot of work has been done in order to accommodate t logic circuits operating at low supply voltage(V_{dd}) V_{dd} scaling is, However, obstructed by the minimum operating voltage (V_{ddmin}) of CMOS logic gates. [1]. $V_{dd(min)}$ is the minimum supply voltage that a logic circuit can tolerate without any damage & with increase in logic gates and CMOS technology down scaling becomes possible , this can achieved by varying channel length of transistors in such a way that for achieving ultra-low power (< 0.4 V) logic circuits $V_{dd(min)}$is reducedWith transistor channel length ranging from 25 nm to 40 nm in size (25 to 40 billionth of a meter), i.e, 45 nm technology which is truly a nanotechnology. For more details table 2 of [2] can be referred, that shows reduction in supply voltages with appropriate changes in channel length. So many famous technologies like 90 nm, 65 nm, 45 nm etc. are currently in working state. In this paper, performance of CMOS-XOR and PTL XOR based on 45 nm technology is compared.

In VLSI (Very large scale integration) implementation, major problems are heat dissipation and power consumption. To solve these problems it is required to reduce power supply voltage, switching frequency and capacitance of transistor [3].Area, delay and power dissipation have emerged as the major concerns of designers. The gate delay depends on the capacitive load of the gate. The dominant term in power dissipation of CMOS circuits is the power required to charge or discharges the capacitance in the circuit. Thus, by reducing capacitance we can decrease the circuit delay and power dissipation. Capacitance is in turn a function of logic cells being used in the design. [4].In this paper, comparison of CMOS technology & Pass transistor logic based on 45 nm technology is done by analysing these different techniques with the help of XOR gate. Section I represents a brief introduction about the trends in the field of chip designing and various terminologies used in the paper.

II. LOGIC TYPES

The latest technology used for constructing integrated circuits is Complementary metal–oxide–semiconductor (CMOS). The technology is being used in various digital and analogy logic circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of applications. Logical representation of CMOS is shown in figure 1.

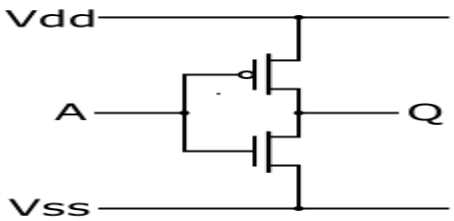

Fig. 1. Logic diagram of CMOS**.**

It is also known as complementary-symmetry metal–oxide–semiconductor (COSMOS) because it uses complementary and symmetrical pairs of both p& n type semiconductor field effect transistor.Two important characteristics of CMOS devices are highnoise immunity and low static power consumption. Since one transistor of the pair is always off , the series combination draws significant power for short duration of time only while switching between on and off states. Also, CMOS devices produce lesser heat in comparison to other forms of logic, e.g., PMOS or NMOS logic. The main reason which made CMOS the most used technology to be implemented in VLSI chips is that, it allows large number of logic functions on a chip.

Another technology used by logic device manufacturers for designing integrated circuit with even lesser number of transistors than CMOS is Pass transistor logic (PTL) .In PTL input is given to both gate and source /drain terminals.These circuits act as switches and uses pair of NMOS and PMOS transistor called Transmission gate & the width of PMOS is taken equal to NMOS so that both transistors can pass the signal simultaneously. Figure 2 shows symbol of pass transistor logic.When g = 0,gb=1 Switch is open &when g=1, gb=0 Switch is closed . So when g=1 : if input is '0' then output will be weak '0' and if input is '1' then output will be strong '1'.

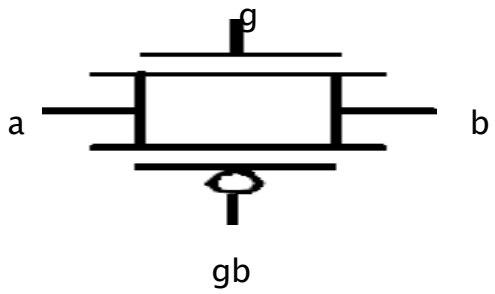

Fig. 2 Pass transistor logic

III. XOR SCHEMATIC &DESIGN

A 2 input XOR gate is designed by using CMOS on MICROWIND/ DSCH3. Figure 3.shows schematic of XOR using CMOS .

Table 1. Function of XOR

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

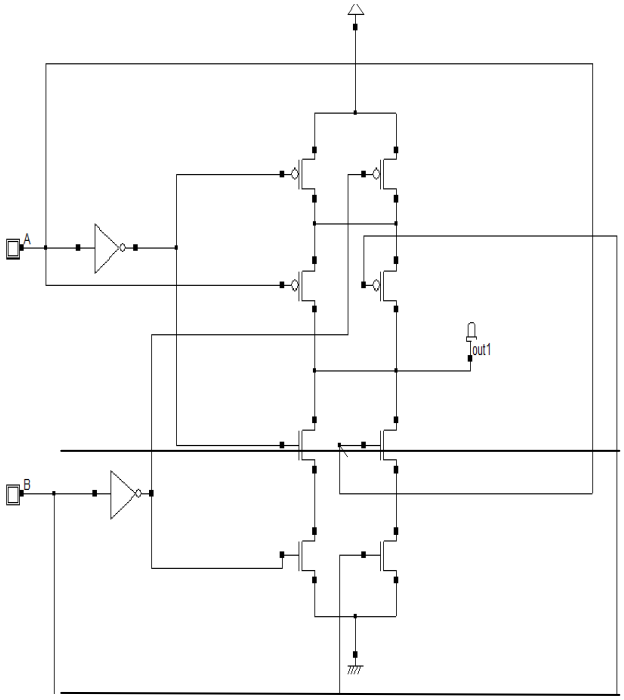

Fig. 3 Schematic of XOR using CMOS logic

Timing diagram of proposed 2 input CMOS XOR is shown in Fig. 5 It logically verifies the different states of the circuit. Timing simulation is performed at schematic design.

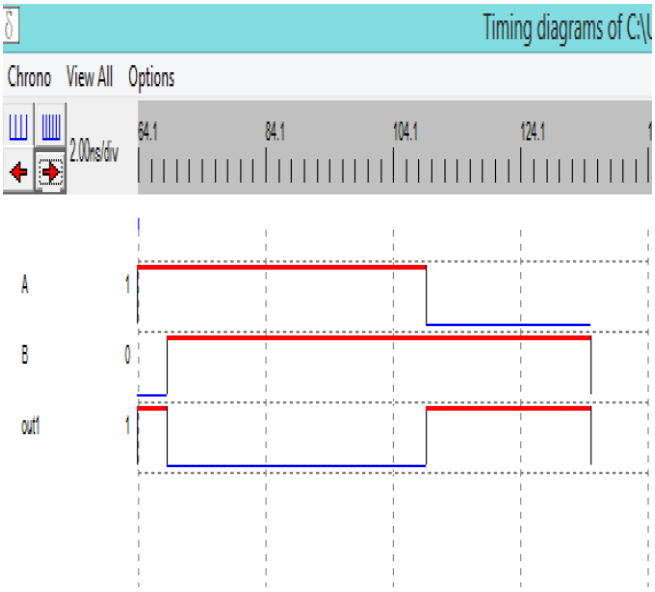

Fig 4 Timing diagram of XOR using CMOS logic

Similarly, schematic of a 2 input XOR gate designed by using Pass transistor on MICROWIND/ DSCH3 is shown in Figure 5 .

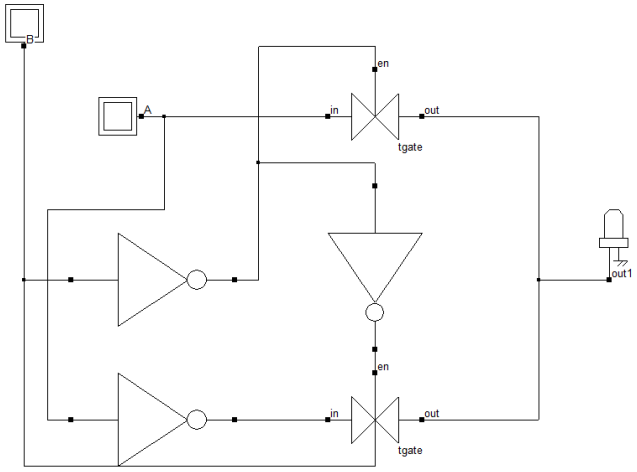

Fig. 5. Schematic of XOR using pass transistor.

Timing diagram of proposed 2 input Pass transistor XOR is shown in Figure 6. It also logically verifies the different states of the circuit. Timing simulation is performed at DSCH3

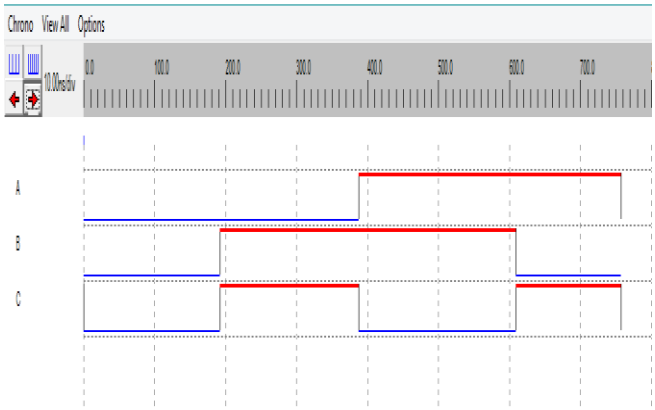

Fig. 6 Timing diagram of XOR using pass transistor

Both the schematics of XOR will work according to the given description in section I & will provide output that is a function of logic XOR.

IV. Layout & Simulation:

In this section, the performance ofXOR logic gate based on CMOS & Pass transistor is evaluated by comparing theirdifferent parameters. All the simulations have been done using Micro wind 3.1 CAD tool[5]. All the Layouts are designed using 45-nm technology with a 0.4 to1.8V supply voltage. Layout design of proposed XOR gates using two different technologies is shown in following figures (7 & 8). Regular layout style is used in order to simplify the overall geometry and the signal routing. Layout occupies the area of 18.8µm^2 for CMOS based XOR & 29µm^2 for Pass transistor based XOR at 45 nm technology shown in Figure 7 & Figure 8 respectively, which shows layout for the proposed design of logic function & simulation results of proposed designs are shown in Figure 9& figure 10.

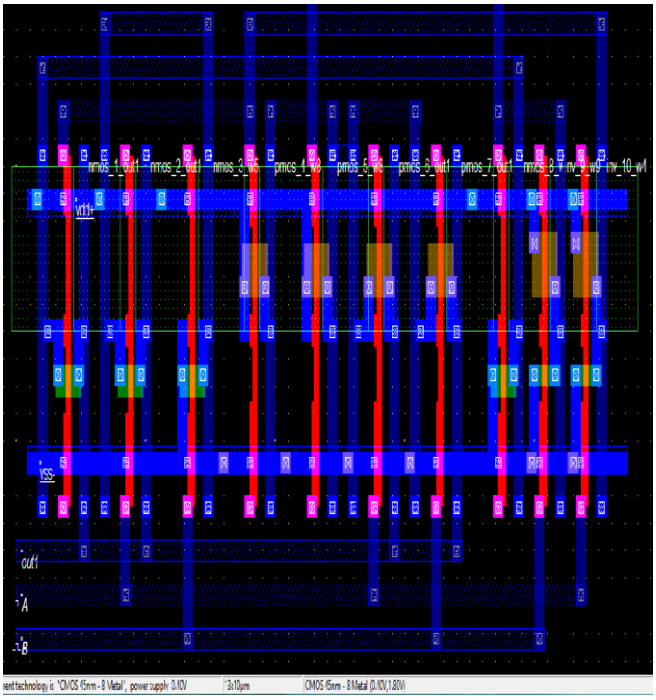

Fig.7 Layout of 45 nm based CMOS XOR gate

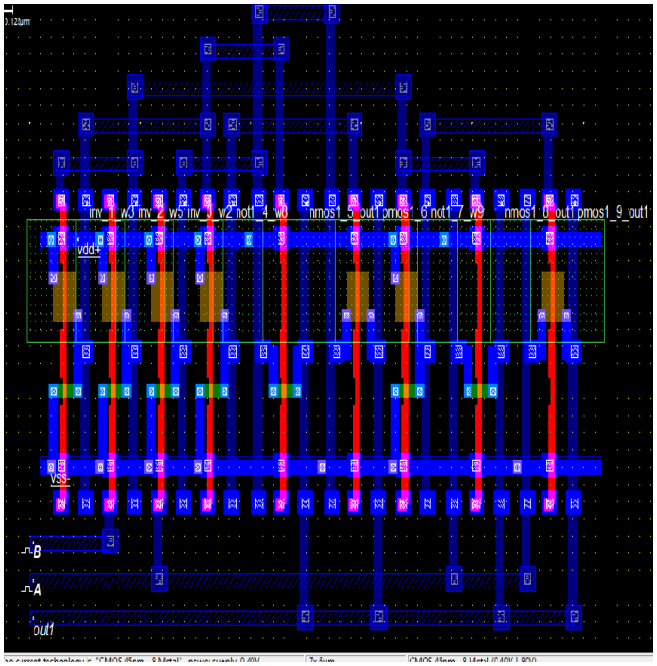

Fig.8 Layout of Pass transistor XOR gate.

Time domain representation of Layout simulations is shown in figure 9 & figure 10. Logic '0' corresponds to a zero voltage and logic '1' corresponds to 0.4 V.

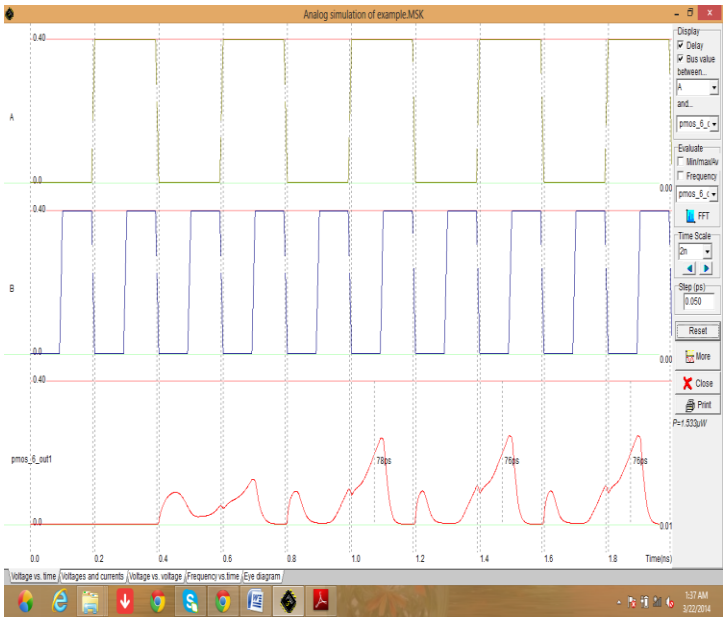

Fig. 9 Layout Simulation of CMOS XOR gate.

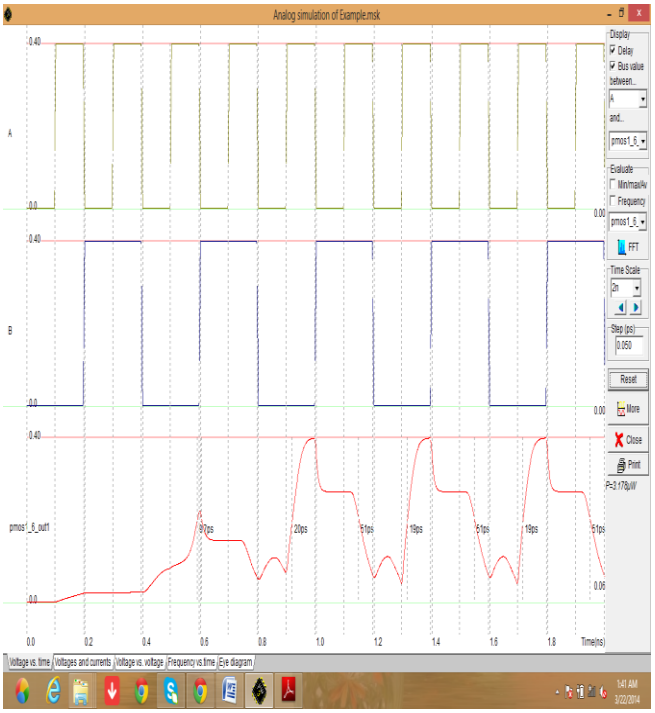

Fig 10 Layout Simulation of Pass transistor logic XOR gate.

V. Results & Comparison:

XOR logic gate based on CMOS & Pass transistor logic is designed on 45 nm technology and compared with each other in terms of various parameters . Simulated results are shown in table 2.

Table 2 . Comparison of simulation results

S.no.	Parameters	CMOS	Pass Transistor
1.	Width of layout	6.1 µm	6.5µm
2.	Height of layout	3.1 µm	4.6 µm
3.	Surface area of layout	18.8µm^2	29.7µm^2
4.	Propagation delay	75 ps	19 ps
5.	Power dissipation	.002 mw	.003 mw
6.	No. of transistors required	12	14

VI. Conclusion:

Both pass transistor logic devices and CMOS technology based devices have their own benefits. The result of

computational comparison shows that pass transistor logic can provide 74.6 % improvement in speed and 57.4% increment in area, therefore acquire more space. Thus, applications where high speed is required PTL based devices are used but applications where size of the chip is priority, CMOS based designs may be preferred.

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